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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,522	07/16/2004	Naoshi Adachi	ABE-025	4666

7590 01/27/2006

Kubovcik & Kubovcik
The Farragut Building
Suite 710
900 17th Street NW
Washington, DC 20006

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·J)

Office Action Summary	Application No.	Applicant(s)	
	10/501,522	ADACHI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment 11/16/05. Currently, claims 16-26 are pending.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16 and 18-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruel, US Patent 5,804,086.

Bruel discloses the semiconductor device and method as claimed. See figures 1A-8, and corresponding text, where Bruel teaches, pertaining to claim 16, a bonded SOI substrate comprising: a SOI layer **12** in which a device is to be formed (figure 3; col. 2, lines 9-12; col. 4, lines 35-39); and a supporting substrate wafer **2** for supporting said SOI layer (figure 2; col. 4, lines 1-4), said SOI layer and said supporting substrate wafer having been bonded to each other **1** with an insulation layer interposed therebetween (col. 2, lines 9-12, ***Note***: the Examiner takes the position that the non-conducting material wafer **12** is an insulating layer and a semiconductor

layer such as silicon), in which said insulation layer has a plurality of cavities defined by different heights (figures 4 and 5; col. 4, lines 18-21 and 40-67; col. 5, lines 1-22, ***Note***: the Examiner takes the position that the thin layer **16** formed on the supporting substrate **2** is an SOI layer, since Bruel teaches that the non-conducting material wafer **12** can include an insulating layer. As a result, the insulating layer having a plurality of cavities defined by different heights is obtained).

Bruel teaches, pertaining to claim 18, a manufacturing method of a bonded SOI substrate, comprising: a recessed portion forming step for forming a recessed portion **10** in a surface of an active layer wafer **12** and/or in a surface of a supporting substrate wafer **2** (figure 2; col., 4, lines 9-20); a bonding step for bonding said active layer wafer and said supporting substrate wafer to each other **1** with said surface(s) having said recessed portion(s) formed therein serving as bonding surface(s) to thereby form a cavity (figure 4; col. 4, lines 36-57); and a thinning step for thinning said active layer wafer of said bonded wafers to thereby form a SOI layer, wherein in said recessed portion forming step, a plurality of recessed portions having varied depth is formed in said surface of said active layer wafer and/or in said surface of said supporting substrate wafer (figures 3-5; col. 4 , lines 40-45).

Bruel teaches, pertaining to claim 19, in which in said bonding step, an insulation film **12** has been formed on said bonding surface of said active layer wafer and/or on said bonding surface of said supporting substrate wafer (figures 4 and 5; col. 4, lines 18-21 and 40-67; col. 5, lines 1-22, ***Note***: the Examiner takes the position that the thin layer **16** formed on the supporting substrate **2** is an SOI layer, since Bruel teaches that the non-conducting material wafer **12** can include an insulating layer).

Bruel teaches, pertaining to claim 20, in which said bonding step is carried out in a vacuum atmosphere or under a vacuum condition (col. 4, lines 50-65, ***Note***: the Examiner takes the position that the bonding step is performed in at least one of a vacuum atmosphere or under a vacuum position, since Bruel teaches the use of conventional gases produced by ion-implantation is performed).

Bruel teaches, pertaining to claim 21, in which said thinning step includes a step of grinding and polishing of said active layer wafer after having been bonded together (col.. 4, lines 40-43).

Bruel teaches, pertaining to claim 22, further comprising a step for performing an ion implantation to a location in a specified depth in said active layer wafer, wherein said thinning step includes, in the course of a heat treatment following to said bonding step, a step for separating a surface side of said active layer wafer from said ion-implanted region (figure 3; 40-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bruel US Patent 5,804,086 in view of Hsu US Patent 6,114,197.

Bruel discloses the semiconductor device substantially as claimed. See preceding rejection of claims 16 and 18-22 under 102(b). In addition, Bruel shows, pertaining to claim 17, said bonded SOI substrate comprising: a SOI layer **1** in which a device is to be formed (figure 1G; col. 8, lines 28-33); and a supporting substrate wafer **6** for supporting said SOI layer (figure 1G; col. 8, lines 28-33, said SOI layer and said supporting substrate wafer having been bonded to each other **7** with an insulation layer **2** interposed therebetween.

However Bruel fails to show, pertaining to claim 17, in which said SOI layer has varied thickness over a plane thereof.

Hsu teaches, a similar device in which includes the SOI layers to have varied thickness over a plane thereof (figure 3, col. 3, lines 1-10).

It would have been obvious to one of ordinary skill in the art to substitute, the step of the SOI layer having varied thickness over a plane thereof, in the method of Bruel, pertaining to claim 17, according to the teachings of Hsu, with the motivation that, by varying the thicknesses of the SOI layers, the surface area of the substrate can be controlled and, as a result, improve the quality of integrated circuits for semiconductor devices.

Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu US Patent US Patent 6,114,197 in view of Bruel US Patent 5,804,086.

Hsu discloses the semiconductor device substantially as claimed. See figures 1-6, and corresponding text, where Hsu shows, pertaining to claim 23, a semiconductor device comprising a bonded SOI substrate **10** in which a SOI layer having varied thickness is formed over a plane thereof (figures 2-3; col. 2, lines 57-64;col. 3, lines 1-10; col. col. 4, lines 1-5),

wherein a functional block defined by a CMOS logic **18** is formed in the thinnest region of said SOI layer and a memory functional block and/or an analog block are formed in the other regions of said SOI layer (figure 6; col. 3, lines 50-60). In addition, Hsu shows, pertaining to claim 24, in which a basic unit block of the CMOS logic is formed in the thinnest region of said SOI layer (figure 6; col. 3, lines 50-60). Also, Hsu shows, pertaining to claim 25, in which a unit transistor is formed in the thinnest region of said SOI layer (figure 6; col. 3, lines 50-60). Finally, Hsu shows, pertaining to claim 26, in which a channel of a unit transistor is formed in the thinnest region of said SOI layer (figure 6; col. 3, lines 50-60).

However, Hsu fails to show, pertaining to claim 23, the step of a cavity being formed at the bonding interface between said SOI layer and said substrate.

Bruel teaches, the formation of cavities within a silicon substrate (figure 2; col. 4, lines 9-20).

It would have been obvious to one of ordinary skill in the art to substitute, the step of a cavity being formed at the bonding interface between said SOI layer and said substrate, in the method of Hsu, pertaining to claim 23, according to the teachings of Bruel, with the motivation that, by forming cavities within the substrate would allow for an increase in the efficiency of heat dissipation required for semiconductor devices.

Response to Arguments

Applicant's arguments with respect to claims 16-26 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
January 14, 2006

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812